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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,739	11/20/2003	Tomoki Ono	245402008000	3121

25226 7590 10/28/2005

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,739	ONO ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgement is made of papers filed under 37 CFR 1.114, claiming priority from U.S. Serial No. 10/719739 filed on which itself claims priority under 35 U.S.C. 1 19(a)-(d), from Japanese Patent Application Nos. 2002-336660 and 2003-376,144 which papers have been placed of record in the file.

Claim Rejections - 35 USC Section 1 03

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action.

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pedains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. (U.S. Patent No. 6,121 ,634, herein after Saito) previously applied and further in view of in view of Yoshida et al. (U.S. Patent No. 5,663,975, herein after Yoshida) .

With respect to claim 1 Saito describes nitride semiconductor light emitting device comprising at least a substrate, (Saito fig. 6A # 200 , col. 8 line 19) an active layer formed of a nitride semiconductor containing mainly In and Ga, (Saito fig. 6A

#205, col. 8 line 24-25) an optical cavity, (inherently present in every LED) a p-electrode(Saito fig. 6A #21 1 , col. 8 lines 32-33) divided into at least two regions, and an n-electrode (Saito figure 6A # 210, col.8 line 32) divided into at least two regions.

Saito does not specifically mention the presently newly added limitation namely wherein a p-electrode divided into at least two regions n-electrode divided into at least two regions and all of said p-electrode and/or said n-electrode regions share the optical cavity.

However, Yoshida , a patent from the same filed of endeavor, describes in figures 1 B , 3C etc. and lines col. 7 lines 50-65, and col.8 lines 55-65 wherein said p-electrode and/or said n-electrode is separated into at least two regions and all of said p-electrode and/or said n-electrode regions share the optical cavity to provide a Led structure with improved heat radiation and effectively prevent heat cross talk with uniform illumination using a thin structure that does not require the use of complicating and expansive elements such as masks or shields or light scattering media and a relatively cheaper chip by decreasing the size and/or the number of chips.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include Yoshida's p-electrode and/or said n-electrode is separated into at least two regions and all of said p-electrode and/or said n-electrode regions share the optical cavity in Saito's device . The motivation for the above combination is to provide a LED structure with improved heat radiation and effectively prevent heat cross talk with uniform illumination using a thin structure that does not require the use of complicating and expansive elements such as masks or shields or

light scattering media and a relatively cheaper chip by decreasing the size and/or the number of chips. (Yoshida col. 1 lines 45-55, col. 4 etc.).

With respect to claim 2 Saito describes the n'ftride semiconductor light emitting diode according to claim 1, wherein said nitride semiconductor light emitting device has self pulsation characteristics. (Saito Abstract lines 4-6, etc.).

With respect to claim 3 Saito describes a nitride semiconductor light emitting device according to claim 1 wherein said active layer has a band gap of at least 2-6 ev (Saito col. 7 line 8-operation voltage 3.8 V) and said nitride semiconductor light emitting device has self pulsation characteristics. (Saito Abstract lines 4-6).

With respect to claim 4 Siato describes the nitride semiconductor light emitting device according to claim 1, wherein said active layer has a band gap of at least 2.6 eV, (Saito col. 7 line 8-operation voltage 3.8 V) and said nitride semiconductor light emitting device has self pulsation characteristics in a light output range of at lease 5 mW.(Saito col. 7 lines 14-16, up to 200mv).

With respect to claim 5 Saito describes the nitride semiconductor light emitting diode according to claim 1.

Saito does not specifically describe the p-electrode and n-electrode are electrically shod-circuited in at least one of the regions of said separated electrode.

However, Yosihda, patent from the same filed of endeavor, describes in figure 9 and col. 11 lines 19-25 describes the p-electrode (drive region first laser resonator) and n-electrode (drive region fourth laser resonator or vice versa) are electrically short-circuited in at least one of the regions of said separated electrode, to provide a common

drive region and a total of operating currents supplied to the respective drive regions and the common drive region is made constant , whereby a temperature of the laser chip can be retained always substantially constant.

Therefore, it would have been obvious to one of ordinary skill in the ad at the time of the invention to include Yoshida's element of the p-electrode (drive region first laser resonator) and n-electrode (drive region fourth laser resonator or vice versa) are electrically short-circuited in at least one of the regions of said separated electrode in Saito's device . The motivation to make the above mentioned inclusion is to provide a

common drive region and a total of operating currents supplied to the respective drive regions and the common drive region is made constant, whereby a temperature of the laser chip can be retained always substantially constant. (Yoshida col. 1 1 lines 19-32).

With respect to claim 6 Saito describes the nitride semiconductor light emitting device according to claim 1 , wherein at least one of said p-electrode and said n-electrode is electrically separated into at least two regions, Yoshida fig.9 , regions 318 a to d) and the p-electrode and n-electrode are electrically shod-circuited in at least one of the regions of said separated electrode, (Yoshida figure 9 and col. 1 1 lines 19-25) and said nitride semiconductor light emitting device has self pulsation characteristics. (Saito Abstract tines 4-6) .

With respect to claim 7 Saito describes the nitride semiconductor light emitting device according to claim 1 , wherein said active layer has' a bandgap of at least 2.6 eV, (Saito col. 7 line 8 operation voltage 3.8 V) and at.least one of said p-electrode and

said n-electrode is electrically separated In to at least two regions (Yoshida fig.9 , regions 318 a to d) and the p-electrode and n-electrode are electrically shod-circuited in at least one of the regions of said separated electrode, (Yoshida col. 1 1 lines 19-25) and said nitride semiconductor light emitting device has self pulsation characteristics. (Saito Abstract lines 4-6).

With respect to claim 8, Saito describes the nitride semiconductor light emitting device according to claim 1 , wherein said active layer has a bandgap of at least 2.6 eV, (Saito col. 7 line 8 operation voltage 3.8 V) and at least one of said p-electrode and said n-electrode is separated electricity into at least two regions, ,(Yoshida fig.9 , regions 318 a to d) and the p-electrode and n-electrode are electrically shod-circuited in at least one of the regions of said separated electrode, and said nitride semiconductor light emitting device has self pulsation characteristics in a light output range of at least 5 mW. (Saito col. 7 lines 14-1 6).

With respect to claim 9, Saito describes the nitride semiconductor light emitting device according to claim 1 , wherein one of said electrodes electrically separated into at least two regions forms contact with one of two mirror facets forming a cavity, (Yoshida figures 9 ,16-22, col. 12 lines 3 to 6, col. 18 lines 7-10) and said mirror facet has a reflection film containing a conductive material, (Yoshida figures 9 ,16-22, col. 12 lines 3 to 6, col. 18 lines 10-16) and the p-electrode and n-electrode are electrically connected by said reflection film. (Yoshida figure 9, col. 12 lines 7-15).

With respect to claim 10 Saito describes the nitride semiconductor light emitting device according to claim 9, wherein one of said electrodes electrically separated into at

least two regions forms contact with one of two mirror facets forming a cavity at a side opposite to an output plane. (Yoshida figures, 16 , etc.).

With respect to claim 11 , Saito describes the nitride semiconductor light emitting device according to claim 9, wherein said conductive material includes Al.(Yoshida col .11 line 57).

With respect to claim 12, Saito describes the nitride semiconductor light emitting device according to claim 1 , wherein a resistor is provided between said p-electrode and said n-electrode in at least one of the regions of said electrode separated into at least two regions. (Yoshida claim 14).

With respect to claim 13, Saito describes the nitride semiconductor light emitting device according to claim 2, wherein self pulsation characteristics are adjusted by said 1resistor provided between said p-electrode and said n-electrode. (Yoshida claim 14).

With respect to claims 14 and 15 , Saito describes the nitride semiconductor light emitting device according to claim 1, wherein Si is added as n type impurities into said active layer, and a concentration of said Si is 1 x 1017/cm3 to 5 Yo 1018/cm3. (Saito col. 6 lines 45-50, conc. Figure 2- Si as n type impurities inherent).

With respect to claim 16, Saito describes the nitride semiconductor light emitting device according to claim 1 ,wherein at least one of said p-electrode and said n-electrode is electricity separated into at least two regions, and the p-electrode and n-electrode are electrically shod-circuited in at least one of the regions of said separated electrode, and a range of 0.02 ', L1/E2 S 0.30 is established, where L1 is a total length of the region where the p-electrode and n-electrode are electrically short-circuited, and

L.2 is a total length of the region not shod-circuited, among the electrode separate, into regions. (Yoshida figures 9, 16 , etc. and col. 18 lines 9-10).

With respect to claims 17 and 18, Saito describes the nitride semiconductor light emitting device according to claim 1, wherein connection is established such that at least one of said electrodes separated into at least two regions has reverse bias applied to said active layer and another of said electrodes separated into at least two regions has forward bias applied to the active layer. (Yoshida description of figures 9, 16 etc-).

Response to Arguments

Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new grounds) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on 8.00 to 5.00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fahmy Wael can be reached on (571) 272-1714.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

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For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven H. Rao

Patent Examiner

October 20, 2005.

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